

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

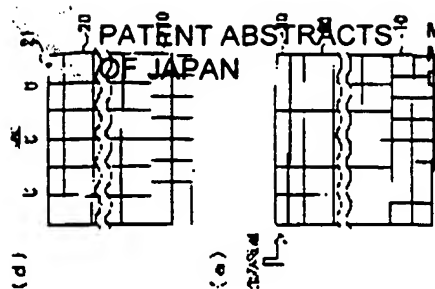
Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

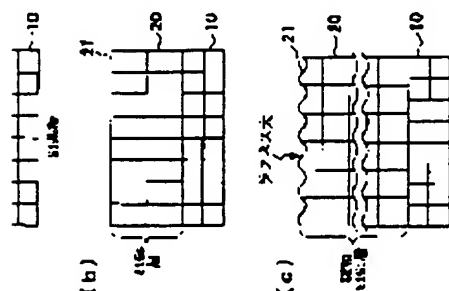
- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



PATENT ABSTRACTS OF JAPAN
METHOD FOR POLISHING SURFACE OF SEMICONDUCTOR, 2002-289533- SAWANO KENTARO
METHOD FOR FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE:



(11)Publication number :

2002-289533

(43)Date of publication of application :

04.10.2002

(51)Int.Cl.

H01L 21/205 H01L 21/304

(21)Application number : 2001-087850

(71)Applicant : SAWANO KENTARO
SHIRAKI YASUHIRO
NAKAGAWA KIYOKAZU

(22)Date of filing : 26.03.2001

(72)Inventor : SAWANO KENTARO
SHIRAKI YASUHIRO
NAKAGAWA KIYOKAZU

(54) METHOD FOR POLISHING SURFACE OF SEMICONDUCTOR, METHOD FOR FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for polishing the surface of a semiconductor in which surface roughness can be reduced while suppressing through dislocation, a method for fabricating a semiconductor device and a semiconductor device.

SOLUTION: On the surface 11 of an Si substrate 10, an SiGe layer 20 having a lattice constant different from that of the Si substrate 10 is grown. The SiGe layer 20 is formed by graded composition buffer method until it has a sufficient thickness and then growth is relaxed. Subsequently, the surface of the SiGe layer 20 is polished by CMP where roughness on the surface 21 of the SiGe layer 20 can be decreased as low as several nm in RMS value. Since Si is grown on a planarized surface 21, a strained Si layer 30 having high planarity can be obtained. In the strained Si layer 30, through dislocation is suppressed and surface roughness is reduced.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

CLAIMS

[Claim(s)]

[Claim 1] The semiconductor surface-lapping method characterized by having the following step.

(a) The step which grows up the 2nd semiconductor with which this 1st semiconductor differs from a lattice constant on the front face of the 1st semiconductor, the step which makes the 2nd semiconductor of (b) above ease, the step which grinds the front face of the 2nd semiconductor of (c) above by the CMP method.

[Claim 2] The 1st semiconductor of the above is the semiconductor surface-lapping method according to claim 1 characterized by consisting of Si.

[Claim 3] The 2nd semiconductor of the above is the semiconductor surface-lapping method according to claim 1 or 2 characterized by consisting of SiGe.

[Claim 4] The 2nd semiconductor of the above is the semiconductor surface-lapping method according to claim 1 to 3 characterized by being formed by the inclination composition buffer method.

[Claim 5] It is the semiconductor surface-lapping method given in any 1 term of the claims 1-4 characterized by carrying out the 5000A or more laminating of the 2nd semiconductor of the above to the front face of the 1st semiconductor of the above in the aforementioned step (a).

[Claim 6] The manufacture method of the semiconductor device characterized by manufacturing a semiconductor device by growing up the 3rd semiconductor into the front face of the 2nd semiconductor of the above ground by the semiconductor surface-lapping method in any 1 term of claims 1-5.

[Claim 7] It is the semiconductor device which is a semiconductor device which comes to carry out the laminating of the 3rd semiconductor which has distortion on the front face of the 2nd semiconductor, and is characterized by the roughness of the front face of the 2nd semiconductor of the above being less than [RMS=10nm].

[Claim 8] The roughness of the front face of the 2nd semiconductor of the above is a semiconductor device according to claim 7 characterized by being less than [RMS=1nm].

[Claim 9] The thickness of the 2nd semiconductor of the above is a semiconductor device according to claim 7 or 8 characterized by being 500A - 1 micrometer.

[Claim 10] The thickness of the 2nd semiconductor of the above is a semiconductor device according to claim 9 characterized by being 1000A or more.

[Claim 11] The thickness of the 2nd semiconductor of the above is a semiconductor device according to claim 9 or 10 characterized by being 5000A or less.

[Claim 12] The manufacture method of the semiconductor device characterized by manufacturing a semiconductor device using the 2nd semiconductor ground by the semiconductor surface-lapping method in any 1 term of claims 1-5.

[Claim 13] The semiconductor device manufactured by the manufacture method of a semiconductor device according to claim 6 or 12.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor surface-lapping method, the manufacture method of a semiconductor device, and a semiconductor device.

[0002]

Background of the Invention] With the detailed-ized technology which progresses every year, ULSI became the high integration and accelerable and has contributed to realization of today's highly informative society. In ULSI, since many Si-MOSFET (Metal Oxide Semiconductor Field Effect Transistor, MOS electric field effect type transistor) produced on (Silicon Si) substrate are used, research towards detailed-ization of Si-MOSFET has been done briskly. However, it is inevitable that a limitation visits to the detailed-ization from now on, and the research which raises the degree of electron transfer which is bearing operation of MOSFET is progressing towards the further improvement in the speed. In MOSFET using GaAs, such an attempt is already made by material and MOSFET in which electronic high-speed movement is possible is put in practical use. However, Si exists abundantly on the earth rather than Ga or As, is cheap and, moreover, has the outstanding feature that no damage done to a human body or environment is. Therefore, the usefulness is large if high-speed MOSFET is producible on Si substrate.

[0003] Then, the method of using as follows SiGe which is the mixed crystal which mixed germanium (germanium) with Si was invented. If Si is made to deposit on SiGe with the larger interatomic distance (lattice constant) than Si (growth), Si layer (distortion Si layer) from which the interatomic distance differs in a direction and the growth (length) direction in a field (width) is produced, and it turns out that mobility goes up the electron in it. Then, realization of distortion Si-MOSFET which uses this distortion Si layer as the channel (path as an electron) of MOSFET is expected. In addition, high-speed operation is expected and MOSFET which uses distortion SiGe and distortion germanium as a channel is also studied.

[0004] In order to produce high-speed MOSFET which introduced these distortion on Si substrate, it is required to be common in all and to grow up a "distortion relief SiGe buffer layer" on Si substrate. It is distorted to drawing 7 and the method of producing Si is shown typically. If SiGe is made to deposit gradually on the crystal Si substrate 1 shown in this drawing (a) (this drawing b), it will grow up with the same lattice constant as Si in the beginning. It is made to grow up furthermore, and if thickness with the SiGe layer 2 is exceeded, it will return to the lattice constant of original of SiGe (this is called relief.). Refer to drawing 5 c. Then, on the eased SiGe layer (a "distortion relief SiGe buffer layer" or a "buffer

layer" only occurs below.) 2, Si is grown up, it deposits and the Si layer 3 is formed. Since this Si layer 3 grows with the same lattice constant as SiGe, it turns into a distortion Si layer. If MOSFET is produced using this distortion Si layer 3, distortion Si-MOSFET will be completed. By this method, in order for the process itself which produces MOSFET not to change at all with the case of MOSFET on mere Si substrate, it has the advantage that this production is easy.

[0005] Thus, in order to realize a SiGe system high-speed device like distortion Si-MOSFET which introduced distortion into the channel, the good distortion relief SiGe layer buffer layer 2 is required. However, since the front face of a buffer layer 2 exists with distortion relief with high density[the increase of roughness (irregularity), and the penetration transposition to which it extends even in a channel], the degree of electron transfer in a channel will fall remarkably. Then, various methods of producing a distortion relief SiGe buffer layer are tried. But common practice is the inclination composition buffer method for raising germanium concentration of a SiGe layer gradually. However, if penetration transposition is stopped, surface roughness will become large, there is an inclination for penetration dislocation density to go up if it is going to make a front face flat, and the buffer grown method which can reduce both surface roughness and penetration dislocation density does not yet exist. Although there is the other low-temperature buffer method for the ability to stop surface roughness sharply, this also has the problem that penetration dislocation density is large.

[0006]

[Problem(s) to be Solved by the Invention] this invention was made in view of the aforementioned situation, and the purpose is offering the semiconductor surface-lapping method which can make surface roughness small, the manufacture method of a semiconductor device, and a semiconductor device, stopping penetration transposition.

[0007]

[Means for Solving the Problem] Corresponding to this technical problem, the semiconductor surface-lapping method according to claim 1 has the following step.

(a) The step which grows up the 2nd semiconductor with which this 1st semiconductor differs from a lattice constant on the front face of the 1st semiconductor, the step which makes the 2nd semiconductor of (b) above ease, the step which grinds the front face of the 2nd semiconductor of (c) above by the CMP method.

[0008] The semiconductor surface-lapping method according to claim 2 shall consist the 1st semiconductor of Si in a thing according to claim 1.

[0009] The semiconductor surface-lapping method according to claim 3 shall consist the 2nd semiconductor of SiGe in a thing according to claim 1 or 2.

[0010] In the thing according to claim 1 to 3, it was presupposed to the semiconductor surface-lapping method according to claim 4 that the 2nd semiconductor is formed by the inclination composition buffer method. Here, the inclination composition buffer method means the crystal-growth method which is made to carry out change elevation of the ratio of the accessory constituent to a principal component

gradually, and goes.

[0011] The semiconductor surface-lapping method according to claim 5 is a thing given in any 1 term of claims 1-4, and the 5000Å or more laminating of the 2nd semiconductor of the above is carried out to the front face of the 1st semiconductor of the above in the step (a).

[0012] The manufacture method of a semiconductor device according to claim 6 manufactures a semiconductor device by growing up the 3rd semiconductor into the front face of the 2nd semiconductor of the above ground by the semiconductor surface-lapping method in any 1 term of claims 1-5.

[0013] A semiconductor device according to claim 7 is a semiconductor device which comes to carry out the laminating of the 3rd semiconductor which has distortion on the front face of the 2nd semiconductor, and the roughness of the front face of the 2nd semiconductor of the above has been less than [RMS=10nm].

[0014] In the thing according to claim 7, the roughness of the front face of the 2nd semiconductor of the above of the semiconductor device according to claim 8 has been less than [RMS=1nm].

[0015] In the thing according to claim 7 or 8, the thickness of the 2nd semiconductor of the above of the semiconductor device according to claim 9 has been 500Å - 1 micrometer.

[0016] In the thing according to claim 9, the thickness of the 2nd semiconductor of the above of the semiconductor device according to claim 10 has been 1000Å or more.

[0017] In the thing according to claim 9 or 10, the thickness of the 2nd semiconductor of the above of the semiconductor device according to claim 11 has been 5000Å or less.

[0018] The manufacture method of a semiconductor device according to claim 12 has the composition of manufacturing a semiconductor device using the 2nd semiconductor ground by the semiconductor surface-lapping method in any 1 term of claims 1-5.

[0019] The semiconductor device according to claim 13 has composition manufactured by the manufacture method of a semiconductor device according to claim 6 or 12.

[0020]

[Function] If flattening of the large buffer-layer front face of roughness can be carried out by polish, both penetration dislocation density and surface roughness can obtain a low distortion relief SiGe buffer layer. Flattening of the front face can be carried out by grinding the sample produced by the inclination composition buffer method with Chemical Mechanical Polishing technology (CMP).

[0021]

[Embodiments of the Invention] The semiconductor surface-lapping method, the manufacture method of a semiconductor device, and semiconductor device concerning 1 operation gestalt of this invention are explained below. First, the polish method is explained based on drawing 1 .

[0022] First, the SiGe layer (the 2nd semiconductor) 20 which is the semiconductor with which this Si substrate 10 and lattice constant differ from each other on the front face 11 of the Si substrate (the 1st semiconductor) 10 shown in drawing 1 (a) is grown up (drawing 1 b). As this growth method, arbitrary

things, such as CVD and the gas source MBE method, can be used. Since the growth method itself is the same as usual, detailed explanation is omitted. Here, although Si was used as composition of the 1st semiconductor with this operation gestalt, otherwise, it is possible to use germanium. Moreover, the SiGe layer 20 is formed by the inclination composition buffer method here. Make start germanium concentration into 0%, and germanium concentration is made to specifically increase by the fixed coefficient, and it controls and forms so that termination (upper limit) germanium concentration may be made into the purpose concentration (30% of for example, germanium concentration). From the former, since such a formation method is well-known, it omits detailed explanation.

[0023] Subsequently, the SiGe layer 20 is grown up until it becomes sufficiently thick, and the SiGe layer 20 is made to ease. As for the thickness of the SiGe layer 20, with this operation gestalt, considering as 5000A or more is desirable. Thereby, the SiGe layer 20 becomes an original lattice constant. Then, irregularity arises in the front face 21, and roughness becomes large on it (drawing 1 c). In addition, it does not pass over the irregularity shown in drawing 1 to what was shown notionally, but, as for the period, it is general that it is larger than a lattice constant. It is the same as that of the conventional technology fundamentally so far.

[0024] Subsequently, the front face 21 of the SiGe layer 20 is ground by the CMP method (drawing 1 d). Although the thing which made the alkali solution of pH 10.5-11, pH 11[for example,], distribute 30nm - 80nm of mean particle diameters, for example, 70nm colloidal silica, can be used as composition of the slurry used for polish, it is not limited to this. The range of 500A - 1 micrometer of thickness of the SiGe layer 20 after polish is 1000A or more or 5000A or less further preferably. Since the CMP polish methods other than the above are the same as usual, detailed explanation is omitted.

[0025] According to the method of this operation gestalt, by this CMP polish, the roughness of the front face 21 of the SiGe layer 20 can be reduced in an RMS value to 10nm or less (the example of an experiment mentioned later 1nm or less) by spending a certain amount of polish time (for example, about 10 minutes). RMS is the standard deviation of measured value (equivalent to surface height), and can be obtained here by taking the sum about all point of measurement, dividing the square of (an average of measured-value-all measured value) by the number of the fixed points a side, and taking the square root of the **.

[0026] Thus, by growing up Si into the front face 21 by which flattening was carried out, the high distortion Si layer 30 of flatness can be obtained. The growth method of this distortion Si layer 30 itself is the same as usual. in the Prior art, when penetration dislocation density tended to go up when flattening of the front face 21 of the SiGe layer 20 tended to be carried out, and it was going to lower penetration dislocation density, the thing with the relation that the roughness of a front face 21 increases for which it accumulates and the roughness of a front face 21 is lowered enough was difficult. On the other hand, according to the method of this operation gestalt, the SiGe layer 20 can be grown up so that penetration dislocation density may become low, and the irregularity of the front face 21 produced as a result can be lowered to the RMS value equivalent to a number atomic layer by the CMP

method. Therefore, penetration dislocation density is low and there is an advantage that the front face 21 which fully has low roughness can be obtained. Therefore, the Si layer 30 by which the laminating was carried out on this front face 21 will have high flatness.

[0027] MOS-FET (semiconductor device) is producible by making the gate, the source, and a drain in the Si layer 30 formed as mentioned above. Since this production method itself is the same as usual, explanation is omitted. Thus, since the flatness of the Si layer 30 used as a channel is high according to constituted MOS-FET, there is an advantage that there is little dispersion of a carrier and it can raise the mobility. Then, the high-speed semiconductor device by Si even if it does not use GaAs can be obtained, and the advantage is large also in respect of cost or safety. Furthermore, since it is realizable with the easy step in comparison, each method of this operation gestalt also has the advantage that operation is easy.

[0028] In addition, although [the aforementioned operation gestalt] a semiconductor device is produced using the distortion Si layer 30, it is also possible to consider as a semiconductor device by making a channel, the gate, and the source to SiGe layer 20 eased the very thing.

[0029]

[Example(s) of Experiment] (Experiment conditions) It experimented on the same experiment conditions as said operation gestalt. Still more detailed conditions are shown below.

(1) composition [of the SiGe layer 20]: -- (4) during composition (3) polish time: 10 minutes polish thickness (polish thickness): to which start germanium concentration made the alkali solution of pH 11 distribute the colloidal silica of 70nm of composition: mean particle diameters of the composition (2) slurry from which termination (upper limit) germanium concentration becomes 30% (Remainder Si and unescapable impurity) 0% by the inclination composition buffer method -- 100nm [0030] It ground the above condition. The result is shown in drawing 2 . Among drawing, (a) shows the front face of the SiGe layer before polish, and (b) shows the front face after polish among drawing. Clearly, it turns out that flatness is improving sharply.

[0031] In addition, according to this invention person's experimental result, the relation between polish thickness and surface roughness came to be shown in drawing 3 . This result shows that very high flatness [say / RMS=0.5nm] can also be realized.

[0032] In addition, the abrasive material has adhered in large quantities, and if optimal washing is not performed, a good epitaxial film cannot carry out regrowth of the polish front face after CMP on it. Then, this invention persons removed adhesion particle completely by washing which used the surfactant. In order that washing might dip a polish front face in 1:1.ammonia:hydrogen-peroxide:water =5:70 70-degree C mixed solution for 10 minutes and might stop the reattachment of particle after that, the rinse of it was carried out by the ultrapure water which added the organic sulfonic acid 0.1%, and it performed the over flow rinse for 10 minutes by ultrapure water further. Next, it dipped in fluoric acid for 30 seconds 0.5% for oxide-film removal. In addition, in order to prevent the reattachment of the particle which remained in the inside of an oxide film, or the front face, the organicsulfonic acid was added also

to fluoric acid 0.1%. Drawing 4 shows a washing result, this drawing (a) is before washing and this drawing (b) is a surface AFM image after washing. It turns out that particle is completely removed by washing.

[0033] In order to perform such washing after CMP and to remove metal contamination and organic substance contamination further, after performing sulfuric-acid hydrogen-peroxide-solution washing, SiGe was grown up again. The photoluminescence was observed from the quantumwell which this constituted. Therefore, the good EPI film was able to be grown up on the polished surface. Moreover, it was checked that the front face of the SiGe film which carried out regrowth is also the RMS value of 1nm or less. That is, it succeeded in obtaining a SiGe (it setting to upper limit and being germanium30%) buffer layer with flatness which was not able to be produced until now and which is called the surface RMS roughness value of 1nm or less.

[0034] Furthermore, as a result of investigating about the polishing pressure force and polish speed, a relation like drawing 5 was obtained. Polish speed was proportional to the polishing pressure force mostly, and it turns out that it is so quick that germanium concentration of SiGe is so large that the particle size of an abrasive material is large. Although it is necessary to change the suitable polishing pressure force arbitrarily by germanium concentration of a sample, the roughness before polish, and the abrasive material, it is thought that $2[100-800g / l]$ is / cm / suitable for it.

[0035] Furthermore, this invention person ground various samples and investigated the difference in the attainment flatness by the sample (drawing 6). Consequently, it is thought that it depends for attainment flatness on the surface-discontinuity density (it is thought that it is proportional to the surface roughness after SEKOETCHI) of a buffer layer greatly. that is, the thing for which a buffer layer from which the roughness after SEKOETCHI performed after CMP is set to 5nm or less is produced in order to obtain the front face not more than RMS roughness 1nm -- it is thought that it is desirable It is expected that the best polish corresponding to crystal-defect density is realizable by furthermore adjusting pH of an abrasive material.

[0036] In addition, the publication of the aforementioned operation form and an example is not what did not pass to a mere example but showed indispensable composition to this invention. The composition of each part will not be restricted above, if the meaning of this invention can be attained.

[0037]

[Effect of the Invention] According to this invention, the semiconductor surface-lapping method which can make surface roughness small, the manufacture method of a semiconductor device, and a semiconductor device can be offered, stopping penetration dislocation.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the semiconductor surface-lapping method, the manufacture method of a semiconductor device, and a semiconductor device.

[0002]

Background of the Invention] With the detailed-ized technology which progresses every year, ULSI became the high integration and accelerable and has contributed to realization of today's highly informative society. In ULSI, since many Si-MOSFET (Metal Oxide Semiconductor Field Effect Transistor, MOS electric field effect type transistor) produced on (Silicon Si) substrate are used, research towards detailed-ization of Si-MOSFET has been done briskly. However, it is inevitable that a limitation visits to the detailed-ization from now on, and the research which raises the degree of electron transfer which is bearing operation of MOSFET is progressing towards the further improvement in the speed. In MOSFET using GaAs, such an attempt is already made by material and MOSFET in which electronic high-speed movement is possible is put in practical use. However, Si exists abundantly on the earth rather than Ga or As, is cheap and, moreover, has the outstanding feature that no damage done to a human body or environment is. Therefore, the usefulness is large if high-speed MOSFET is producible on Si substrate.

[0003] Then, the method of using as follows SiGe which is the mixed crystal which mixed germanium (germanium) with Si was invented. If Si is made to deposit on SiGe with the larger interatomic distance (lattice constant) than Si (growth), Si layer (distortion Si layer) from which the interatomic distance differs in a direction and the growth (length) direction in a field (width) is produced, and it turns out that mobility goes up the electron in it. Then, realization of distortion Si-MOSFET which uses this distortion Si layer as the channel (path as an electron) of MOSFET is expected. In addition, high-speed operation is expected and MOSFET which uses distortion SiGe and distortion germanium as a channel is also studied.

[0004] In order to produce high-speed MOSFET which introduced these distortion on Si substrate, it is required to be common in all and to grow up a "distortion relief SiGe buffer layer" on Si substrate. It is distorted to drawing 7 and the method of producing Si is shown typically. If SiGe is made to deposit gradually on the crystal Si substrate 1 shown in this drawing (a) (this drawing b), it will grow up with the same lattice constant as Si in the beginning. It is made to grow up furthermore, and if thickness with the SiGe layer 2 is exceeded, it will return to the lattice constant of original of SiGe (this is called relief.). Refer to drawing 5 c. Then, on the eased SiGe layer (a "distortion relief SiGe buffer layer" or a "buffer layer" only occurs below.) 2, Si is grown up, it deposits and the Si layer 3 is formed. Since this Si layer 3 grows with the same lattice constant as SiGe, it turns into a distortion Si layer. If MOSFET is produced using this distortion Si layer 3, distortion Si-MOSFET will be completed. By this method, in order for the process itself which produces MOSFET not to change at all with the case of MOSFET on mere Si substrate, it has the advantage that this production is easy.

[0005] Thus, in order to realize a SiGe system high-speed device like distortion Si-MOSFET which introduced distortion into the channel, the good distortion relief SiGe layer buffer layer 2 is required. However, since the front face of a buffer layer 2 exists with distortion relief with high density[the increase of roughness (irregularity), and the penetration transposition to which it extends even in a channel], the degree of electron transfer in a channel will fall remarkably. Then, various methods of producing a distortion relief SiGe buffer layer are tried. But common practice is the inclination composition buffer method for raising germanium concentration of a SiGe layer gradually. However, if penetration transposition is stopped, surface roughness will become large, there is an inclination for penetration dislocation density to go up if it is going to make a front face flat, and the buffer grown method which can reduce both surface roughness and penetration dislocation density does not yet exist. Although there is the other low-temperature buffer method for the ability to stop surface roughness sharply, this also has the problem that penetration dislocation density is large.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the semiconductor surface-lapping method which can make surface roughness small, the manufacture method of a semiconductor device, and a semiconductor device can be offered, stopping penetration dislocation.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is explanatory drawing for explaining the manufacturing process of the semiconductor device concerning 1 operation gestalt of this invention.

[Drawing 2] It is the photograph in which the experimental result of the semiconductor surface-lapping method concerning the example of 1 experiment of this invention is shown.

[Drawing 3] It is the graph which shows the experimental result of the semiconductor surface-lapping method concerning the example of 1 experiment of this invention.

[Drawing 4] It is the photograph in which the experimental result of the semiconductor surface-lapping

method concerning the example of 1 experiment of this invention is shown.

[Drawing 5] It is the graph which shows the relation of the polish speed and the polishing pressure force in the example of 1 experiment of this invention.

[Drawing 6] It is a graph for explaining the experimental result of the example of 1 experiment of this invention.

[Drawing 7] It is explanatory drawing for explaining typically the important section of the conventional semiconductor-device manufacturing process.

[Description of Notations]

10 Si Substrate (1st Semiconductor)

11 Front Face of Si Substrate

20 SiGe Layer (2nd Semiconductor)

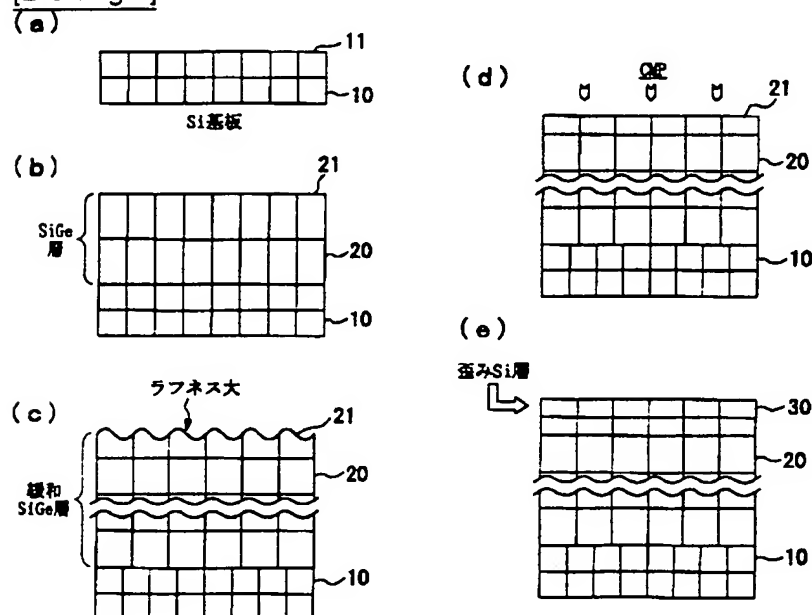
21 Front Face of SiGe Layer

30 Distortion Si Layer (3rd Semiconductor)

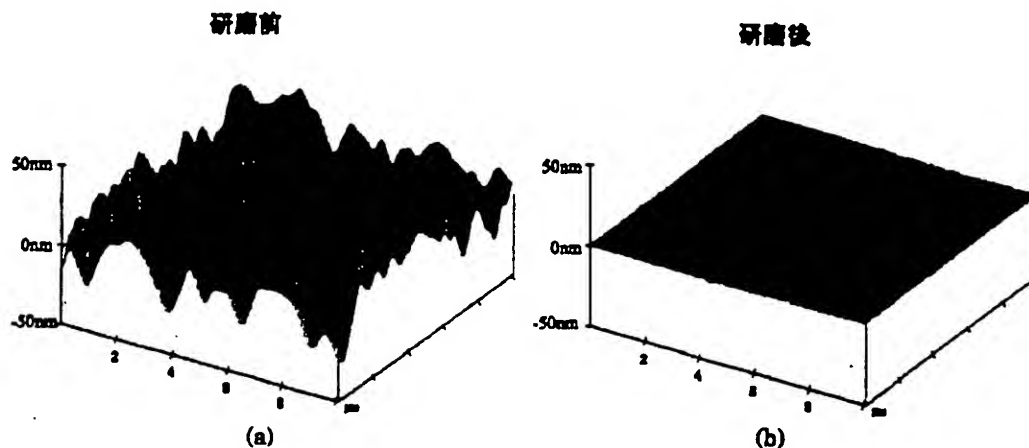
[Translation done.].

DRAWINGS

[Drawing 1]

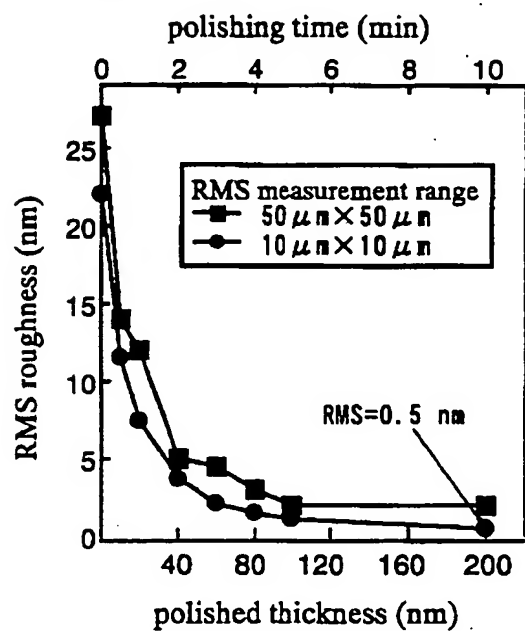


[Drawing 2]



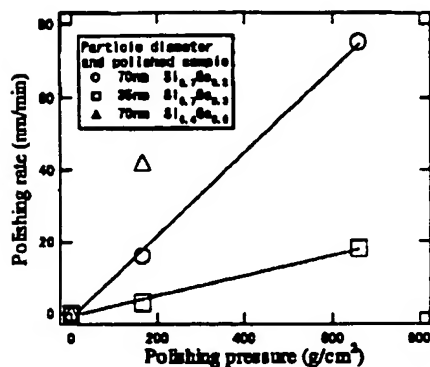
研磨前後の歪み緩和SiGeバッファ層表面のAFM像

[Drawing 3]



研磨膜厚（研磨時間）による RMS ラフネスの変化

[Drawing 5]

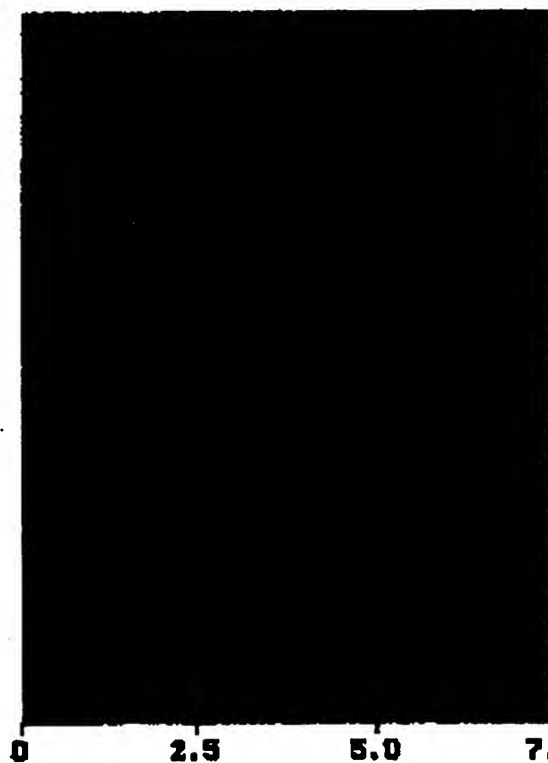
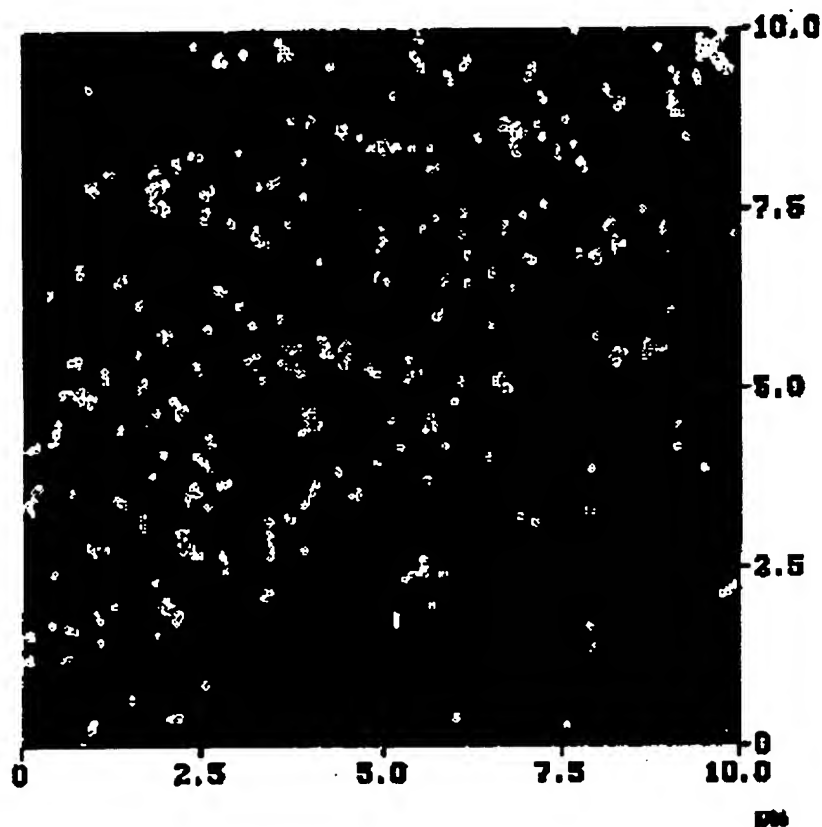


研磨速度と研磨圧力の関係

[Drawing 4]

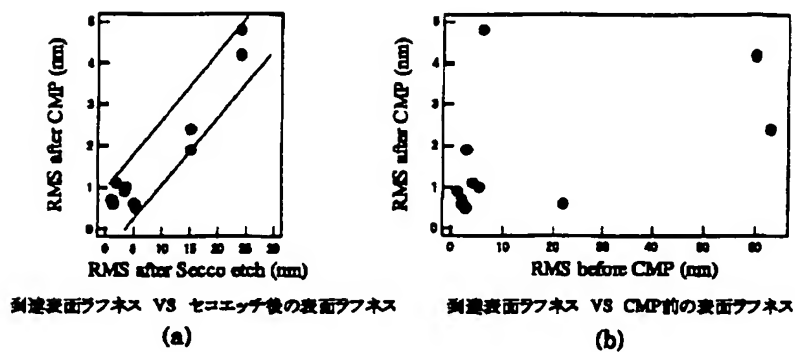
洗浄前

洗浄後

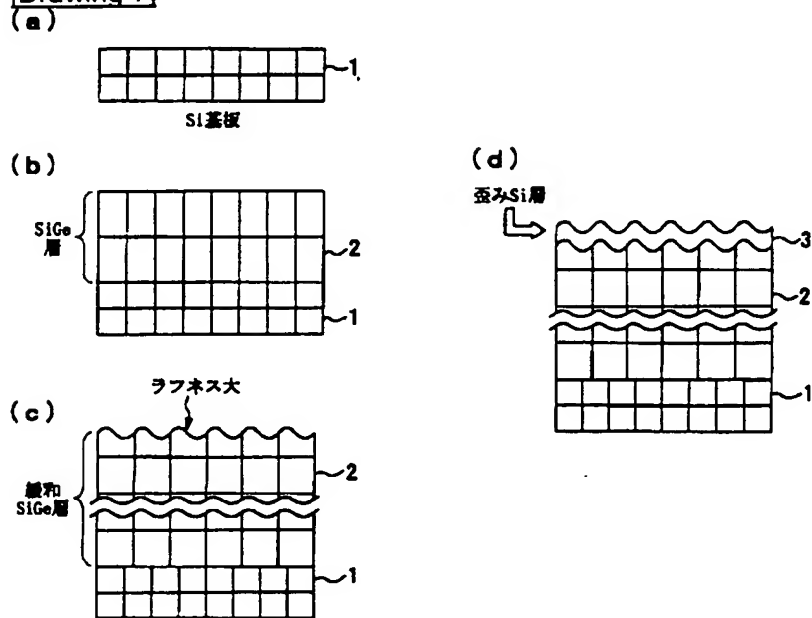


洗浄前後の表面AFM像

[Drawing 6]



[Drawing 7]



[Translation done.]